REMARKS

A proposed correction to FIG. 1 including the legend "PRIOR ART" is attached to satisfy the objection.

New Claims 8-10 have been added. Support for Claims 8-10 may be found in the specification beginning on page 5, line 17 and in FIGS. 2 and 3.

Claims 1-10 remain pending in the application.

Response to the rejection under 35 USC § 102(e) of Claims 1-7

Claims 1-7 stand rejected under 35 USC § 102(e) as being anticipated by Fujimoto et al., U.S. Patent Publication No. US2002/0083352 A1 (*Fujimoto*). Applicant traverses the rejection as follows.

Regarding the rejection of Claims 1-3 in section 2, pages 2 and 3, the rejection errs in alleging that *Fujimoto* discloses placing a level shifter in a pre-selected state if the input power supply is not powered on when the output power supply is powered on as recited in Claims 1-3. Specifically, the rejection alleges that the low voltage generated by the input power supply is equivalent to not being powered on: "the input voltage, such as 1.1 volts, is still at a low level (off-state)". However, if the input power supply is not powered on, it cannot generate 1.1 V as alleged by the rejection. In contrast to *Fujimoto*, Claims 1-3 clearly recite the condition that the input power supply is not powered on. Because *Fujimoto* fails to disclose the condition that the input power supply is not powered on, *Fujimoto* fails to include each and every element recited in Claims 1-3.

Further, *Fujimoto* fails to disclose that the first power supply (*VDD1*) in FIG. 1 controls the state of either the

first level shifter (1) or the second level shifter (2) when the first power supply (*VDD1*) is not powered on and the second power supply (*VDD2*) is powered on. In fact, *Fujimoto* shows in FIGS. 4 and 5 that the states of both the first level shifter (1) and the second level shifter (2) are indeterminate when the first power supply (*VDD1*) is not powered on and the second power supply (*VDD2*) is powered on, because the outputs of the inverters (*IV1*) and (*IV2*) do not generate complementary drive voltages to (*n1*) and (*n2*) when the first power supply (*VDD1*) is not powered on. Because the states of the first level shifter (1) and the second level shifter (2) are indeterminate when the first power supply (*VDD1*) is not powered on, *Fujimoto* fails to disclose placing either the first level shifter (1) or the second level shifter (2) in a pre-selected state when the input power supply is not powered on. Because *Fujimoto* fails to disclose placing either the first level shifter (1) or the second level shifter (2) in a pre-selected state when the input power supply is not powered on, *Fujimoto* fails to include each and every element recited in Claims 1-3.

Further, because *Fujimoto* fails to disclose placing either the first level shifter (1) or the second level shifter (2) in a pre-selected state when the first power supply (*VDD1*) is not powered on, neither the first level shifter (1) or the second level shifter (2) is released from the pre-selected state to follow the input signal (*IN*) when the input voltage is powered on, as alleged by the rejection on page 3. Because *Fujimoto* fails to disclose releasing either the first level shifter (1) or the second level shifter (2) from the pre-selected state to follow the input signal (*IN*) when the input power supply is powered on as recited in Claims 1-3, *Fujimoto* fails to include each and every element recited in Claims 1-3.

Because *Fujimoto* fails to include each and every

element recited in Claims 1-3, the rejection of Claims 1-3 under 35 U.S.C. § 102 lacks reasonable support. Because the rejection lacks reasonable support, Applicant submits that the rejection of Claims 1-3 under 35 U.S.C. § 102 should be withdrawn.

Regarding the rejection of Claims 2-3, the rejection errs in alleging that the claimed steps of connecting a common voltage rail and presenting a high impedance to an output signal port or an inverted output signal port of the level shifter reads on inverting an output signal of a level shifter. As explained in the paragraph beginning on page 6, line 26 of the specification and shown in FIG. 3, the common voltage rail is connected to either the output signal port 104 or the inverse output signal port 106 of the level shifter 100 if the output power supply 204 is powered on when the input power supply 202 is not powered on. Because connecting the common voltage rail to the level shifter 100 when the input power supply 202 is not powered on does not read on inverting an output signal of a level shifter, the rejection fails to meet the recitations of Claim 2. Likewise, connecting a high impedance to the output signal port 104 or the inverse output signal port 106 of the level shifter 100 when the input power supply 202 is powered on as recited in Claim 3 does not read on inverting an output signal of a level shifter, therefore *Fujimoto* fails to include each and every element recited in Claims 2 and 3.

Because *Fujimoto* fails to include each and every element recited in Claims 2 and 3, the rejection of Claims 2-3 under 35 U.S.C. § 102 lacks reasonable support. Because the rejection lacks reasonable support, Applicant submits that the rejection of Claims 2 and 3 under 35 U.S.C. § 102 should be withdrawn.

Regarding the rejection of Claims 4 and 7, the rejection repeats the errors identified above in the rejection of Claims 1-3.

Because *Fujimoto* fails to disclose placing the state of either the first level shifter (1) or the second level shifter (2) in a pre-selected state when the input power supplt (*VDD1*) is not powered on and because *Fujimoto* fails to disclose releasing either the first level shifter (1) or the second level shifter (2) from the pre-selected state to follow the input signal (*IN*) when the input power supply is powered on as recited in Claims 4 and 7, *Fujimoto* fails to include each and every element recited in Claims 4 and 7. Because *Fujimoto* fails to include each and every element recited in Claims 4 and 7, the rejection of Claims 4 and 7 lacks reasonable support. Because the rejection lacks reasonable support, Applicant submits that the rejection of Claims 4 and 7 under 35 U.S.C. § 102 should be withdrawn.

Regarding the rejection of Claims 5 and 6, the rejection repeats the errors identified above in the rejection of Claims 2 and 3.

Because *Fujimoto* fails to disclose the claimed steps of connecting a common voltage rail and presenting a high impedance to an output signal port or an inverted output signal port of the level shifter, *Fujimoto* fails to include each and every element recited in Claims 5 and 6. Because *Fujimoto* fails to include each and every element recited in Claims 5 and 6, the rejection of Claims 5 and 6 under 35 U.S.C. § 102 lacks reasonable support. Because the rejection lacks reasonable support, Applicant submits that the rejection of Claims 5 and 6 under 35 U.S.C. § 102 should be withdrawn.

Applicant respectfully requests examination of

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Claims 1-10 and reconsideration of Claims 1-7.

No additional fee is believed due for this amendment.

Respectfully submitted,

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